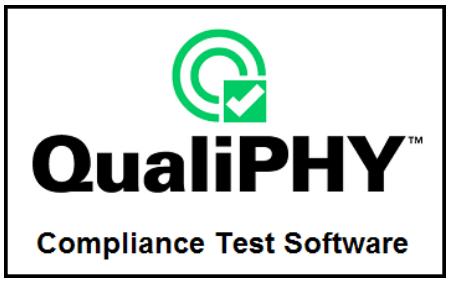


QPHY-PCIe
PCI Express Serial Data
Operator's Manual

Revision A – April, 2008

Relating to the Following Release Versions:

- **Software Option Rev. 5.3**
- **PCIe Script Rev. 1.1**
- **Style Sheet Rev. 1.2**

LeCroy Corporation

700 Chestnut Ridge Road
Chestnut Ridge, NY 10977–6499
Tel: (845) 578 6020, Fax: (845) 578 5985

Internet: www.lecroy.com

© 2008 by LeCroy Corporation. All rights reserved.

LeCroy, ActiveDSO, WaveLink, JitterTrack, WavePro, WaveMaster, WaveSurfer, WaveExpert, WaveRunner and WaveJet are registered trademarks of LeCroy Corporation. Other product or brand names are trademarks or requested trademarks of their respective holders. Information in this publication supersedes all earlier versions. Specifications subject to change without notice.

Manufactured under an ISO 9000 Registered Quality Management System

Visit www.lecroy.com to view the certificate.

This electronic product is subject to disposal and recycling regulations that vary by country and region. Many countries prohibit the disposal of waste electronic equipment in standard waste receptacles.

For more information about proper disposal and recycling of your LeCroy product, please visit www.lecroy.com/recycle.

Document Number: 915746 Rev A

TABLE OF CONTENTS

INTRODUCTION TO QPHY-PCIE 6
Required equipment 6
PCI Express Compliance Test Fixtures 6

QUALIPHY COMPLIANCE TEST PLATFORM 8
Oscilloscope Option Key Installation 10
Typical (Recommended) Configuration 10
Remote (Network) Configuration 10
Oscilloscope Selection 10
Accessing the QPHY-PCIe Software using QualiPHY 11
Customizing QualiPHY 13
QPHY-PCIe Operation 15

INTRODUCTION TO PCI-EXPRESS 16
PCI Express Device Development Process 16
PCI Express Device Development Process and Compliance Tests 17

PCI EXPRESS MEASUREMENT THEORY 18
Eye Pattern and Jitter Measurements 18
Version 1.1 Measurements 18

PCI EXPRESS MEASUREMENT PREPARATION 19
Channel Deskew using Oscilloscope Calibrator Output (SMA Cables) 19
Channel Deskew using Device Under Test Signal (SMA Cables) 21
Differential Probe Calibration 23
For SDA 6000A 24

QPHY-PCIE TEST CONFIGURATIONS 26
All Transmitter tests (with SSC) - system 26
All Transmitter tests (without SSC) - system 26
All Transmitter tests (without SSC) - TX 27
Demo 27
Deskew only 27
Electrical Idle tests 28
Empty Template 28
Initial active link training (add-in card only) 28
Lane To Lane Skew test - add-in card 28
Lane To Lane Skew test - system 28
Reference Clock tests 28
Secondary clock domain test 29
Signal Quality Test - TX 29
Signal Quality Test (CEM) - add-in card 29
Signal Quality Test (CEM) - system (with SSC) 29
SSC Data and Modulation Rate test 29

QPHY-PCIE VARIABLES 30
FormFactor 30
ExecutionOrderMode 30
Deskew value in picoseconds 30
Deskew measure mode method 30
Device type 30
DemoMode 30
Test 1.1 Bit Rate Clock Accuracy Variables 30

Probing method 30
Test 1.5: Signal Quality 30
CleanClock 30
Test 1.7 TX L0 to Electrical Idle to L0 Variables 30
Probing method 30
Test 1.9 RX Detect Hi-Z 30
Probing method 30
Test 1.10 RX Detect Low-Z 31
Probing method 31
Test 1.12 TX Output Rise/Fall 31
Probing method 31
Test 1.16 TX Transitions from Electrical Idle Variables 31
Probing method 31
CleanClock 31
Test 1.18 Initial Active Link Training 31
Probing method 31
Reference Clock Differential Tests 31
Probing method 31
Period: SSC 31

QPHY-PCIE LIMIT SETS 31
PCIe1.1 31

QPHY-PCIE TESTS 31
PCIe 1.1 Script Initialization 31
Test 1.1: Bit Rate Clock Accuracy 31
Test 1.2: SSC TX Data and Modulation Rate 32
Test 1.4: Non-SSC TX Data Rate 32
Test 1.5: Signal Quality 32
Test 1.6: TX DC Common Mode Voltage 33
Test 1.7: TX L0 to Electrical Idle to L0 33
Test 1.8: RX Detect Voltage 33
Test 1.9: RX Detect Hi-Z 33
Test 1.10: RX Detect Low-Z 34
Test 1.11: Lane-to-Lane Skew 34
Test 1.12: TX Output Rise/Fall 34
Test 1.16: TX Transitions from Electrical Idle 35
Test 1.17: Receiver Detection Sequence 35
Test 1.18 Initial Active Link Training 35
Test 1.19: Reference Clock Tests 36
Changes from Version 1.0a 36
Single-Ended Tests 37
Input Voltage 37
Crossing Voltage 37
Rise Fall Matching 38
Differential Tests 39
Edge Rate 39
Differential Voltage 39
Ringback 40
Period 40

TABLE OF FIGURES

Figure 1. Compliance Load Board (CLB) connected to a motherboard 7
Figure 2. Compliance Base Board (CBB) 7
Figure 3. Report menu in QualiPHY General Setup 8
Figure 4. The Test Report includes a summary table with links to the detailed test results 9
Figure 5. QualiPHY main menu and compliance test Standard selection menu 11
Figure 6. QualiPHY configuration selection menu 12
Figure 7. QualiPHY test item selection menu 13
Figure 8. Variable Setup and Limits Manager windows 14
Figure 9. Start button 15
Figure 10. Example of pop-up connection diagram and dialog box 15
Figure 11. PCI Express path to design compliance 16
Figure 12. Example requirements from the PCI Express design checklist 17
Figure 13. Deskew cable setup 19
Figure 14. Deskew control in channel menu: adjust this value to achieve minimum skew 19
Figure 15. Math setup 20
Figure 16. The Skew parameter right side dialog, Skew clock 2 tab, showing default setup 22
Figure 17. Signals properly adjusted for best accuracy 23
Figure 18. Horizontal and memory setup menus properly configured for testing PCI Express signals 24
Figure 19. Selecting signal under test in Serial Data Analysis dialog 25
Figure 20. VCROSS Absolute (From PCI Express CEM 1.1 specification) 37
Figure 21. VCROSS Delta (From PCI Express CEM 1.1 specification) 37
Figure 22. Rise-Fall Matching (From PCI Express CEM 1.1 specification) 38
Figure 23. Fall Edge Rate (From PCI Express CEM 1.1 specification) 39
Figure 24. Ring Back (From PCI Express CEM 1.1 specification) 40
Figure 25. Period (from PCI Express CEM 1.1 specification) 41

INTRODUCTION TO QPHY-PCIE

The New LeCroy PCI Express Development Software for the SDA 6000A, SDA 6020, SDA 9000, SDA 11000 and SDA 13000 serial data analyzers is designed with two major objectives in mind:

- QPHY-PCIe provides the necessary tools to develop PCI Express-compliant devices in a systematic, step-by-step fashion in accordance with revision 1.1 of the specification documents published by PCI-SIG.
- Quick and easy access to all the compliance test requirements from the base and add-in card specifications, and summarized in the Signal Quality Test SIGTEST electrical test tool. LeCroy uses the Intel-certified DLL and integrates the tool into the X-Stream processing software. This enables in-process measurement and reporting of PCI Express critical parameters.

The standard features of the SDA also provide a broad toolset for advanced debugging of these interfaces, including jitter, eye pattern, and bit error rate.

Required equipment

- SDA 6000A, SDA 6020, SDA 9000, SDA 11000 or SDA 13000
- PCI Express Compliance & Development software option (LeCroy QPHY-PCIe)
- 2 matched-length SMA cables for single-ended tests*****
- 2 differential probes
    - D600-type for SDA 6000A, SDA 6020 or SDA 9000
    - D11000PS-type for SDA 11000
    - D13000PS-type for SDA 13000
- 1 SMA T connector
- 1 BNC-to-SMA adapter
- 1 compliance test fixture that is compliant with Rev 1.1 of the Base and CEM Specifications (CLB or CBB as appropriate for testing a system or add-in card)
- A Host computer, though not required, can be used to execute QualiPHY, the Compliance & Development Software Engine.

***Note:** All tests can be performed single ended. This is the recommended configuration.

PCI Express Compliance Test Fixtures

The PCI Express standard describes a set of two fixtures used for connection to the signal under test. The fixtures are known as the compliance load board (CLB) and the compliance base board (CBB). The CLB is used to test system boards, and the CBB is used for testing add-in cards. Both the CLB and CBB are available through the PCI special interest group (PCI-SIG) at www.pcisig.org. Fixtures that are compliant with Revision 1.1 of the Base and CEM Specifications are required to execute QPHY-PCIe tests.

Using SMA type cables, both fixtures allow positive and negative lines attachment of the differential signals directly to separate channels on the instrument. The 50 Ω impedance on each oscilloscope channel provides the proper loading for compliance testing. All PCI Express add-in cards and system boards must transmit a standard compliance pattern when loaded with 50 Ω to ground on each line – all while no signal is being received. The fixtures are designed to apply the compliance test load to the ports of the device under test. The CBB provides a 100 MHz system clock used by add-in cards plugged into the fixture and a socket for a standard ATX power supply.

The compliance load board (CLB) connected to a motherboard. This fixture provides probing access for 1, 4, 8, and 16 lane connectors. The following figure shows the 1 lane section being used. The SMA cables connect the D+ and D- signals to the oscilloscope channels.

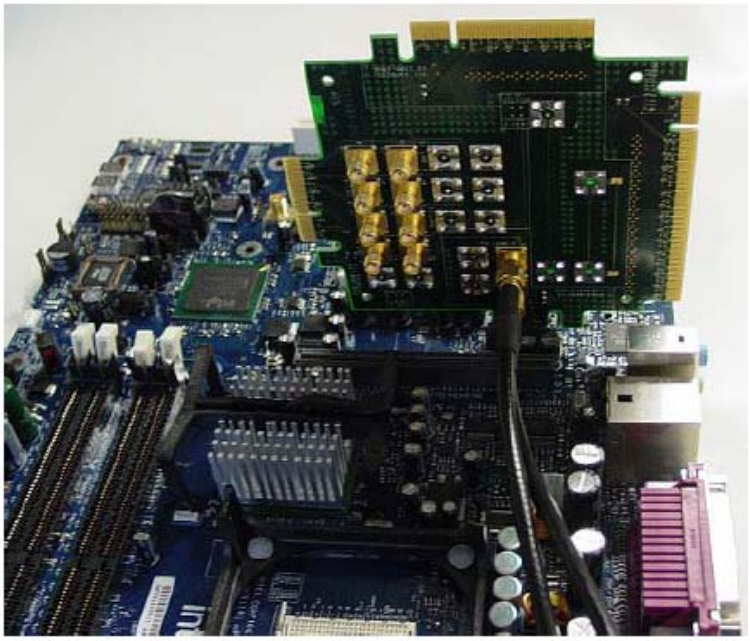


Figure 1. Compliance Load Board (CLB) connected to a motherboard

The compliance base board (CBB) provides a clean reference clock and clock noise injection capabilities.

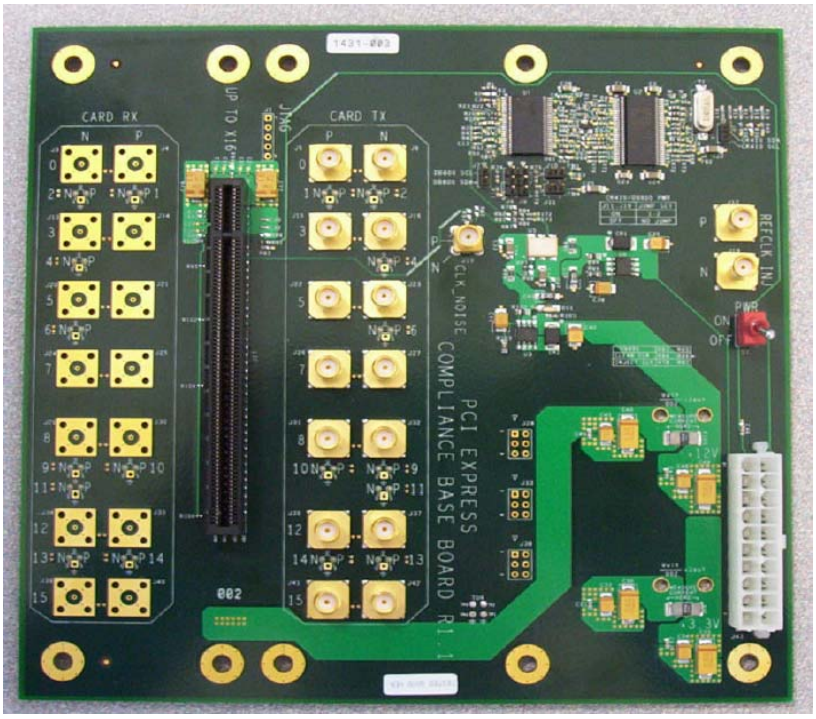


Figure 2. Compliance Base Board (CBB)

QUALIPHY COMPLIANCE TEST PLATFORM

QualiPHY is LeCroy's compliance test framework which leads the user through the compliance tests. QualiPHY displays connection diagrams to ensure tests run properly, automates the oscilloscope setup, and generates complete, detailed reports.

The QualiPHY software application automates the test and report generation.

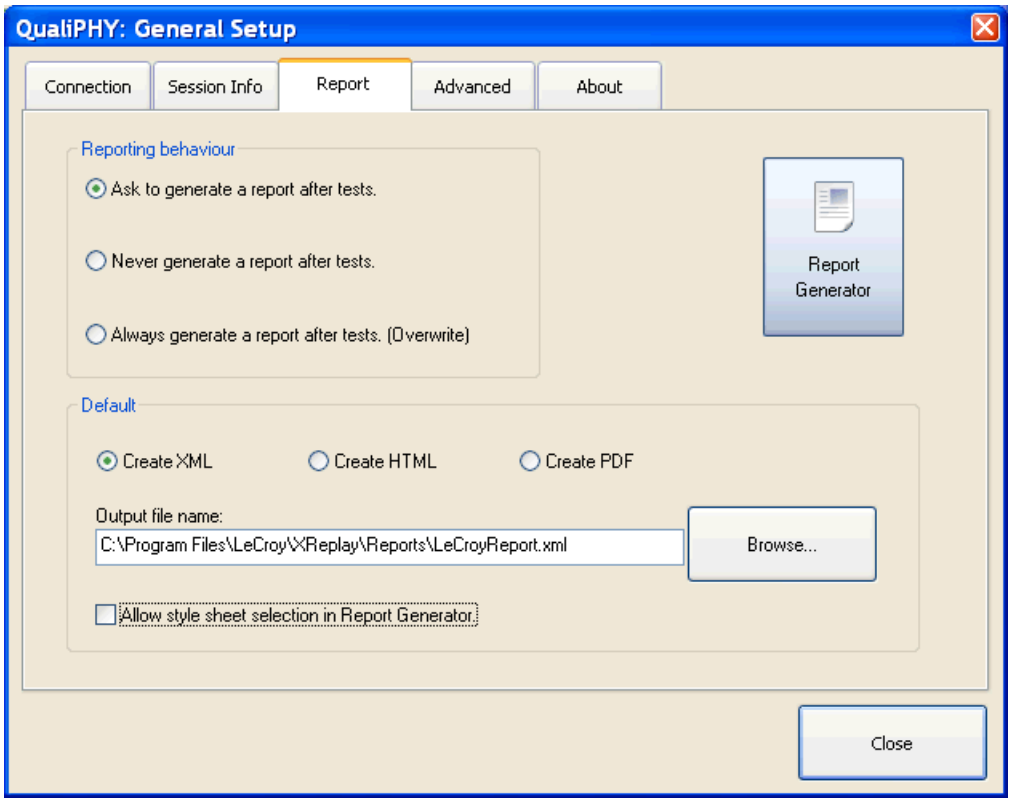
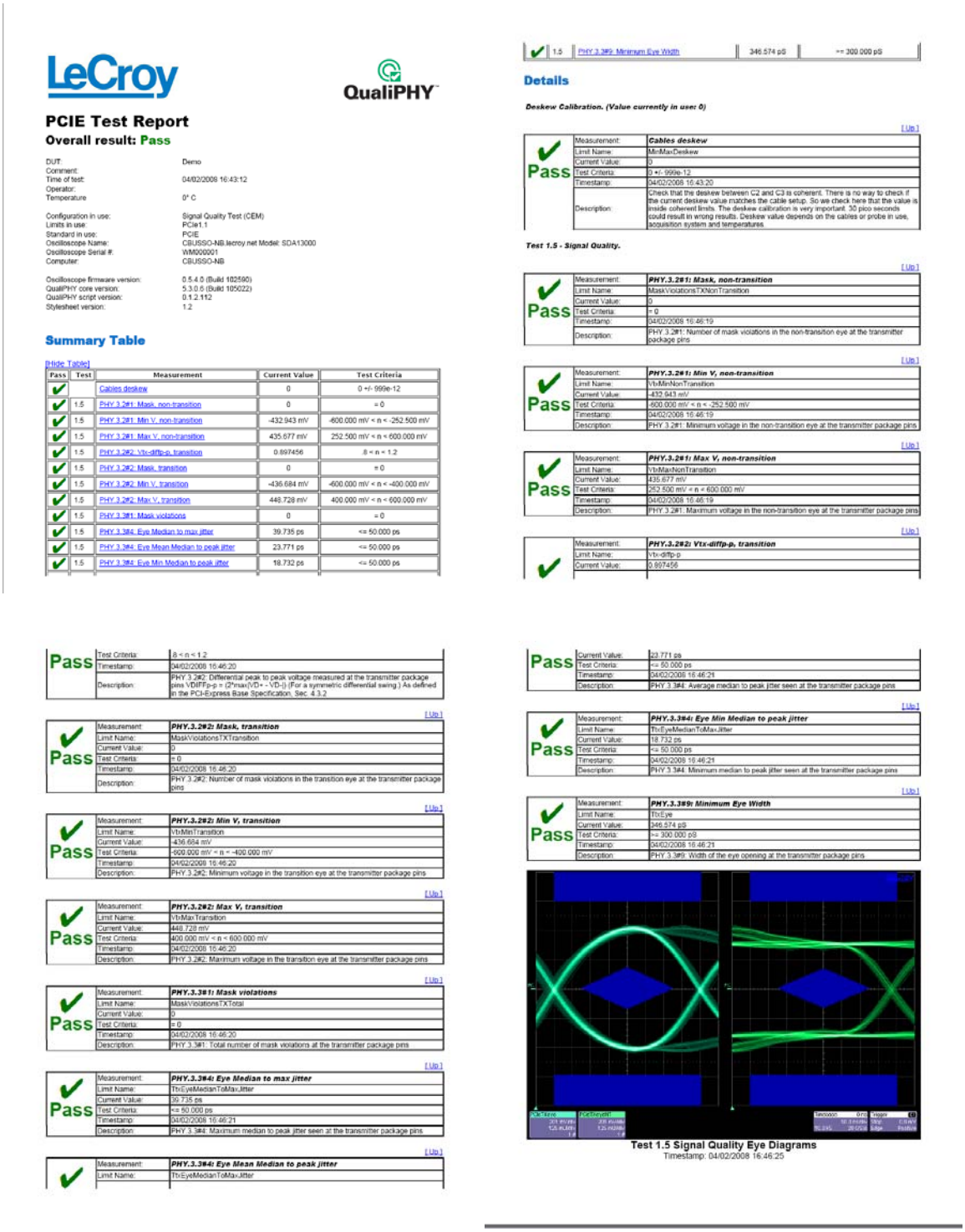


Figure 3. Report menu in QualiPHY General Setup

See the **QualiPHY Operator's Manual** for more information on how to use the QualiPHY framework.



PCIE Test Report

Overall result: Pass

DUT:	Demo
Comment:	
Time of test:	04/02/2008 16:43:12
Operator:	
Temperature	0° C
Configuration in use:	Signal Quality Test (CEM)
Limits in use:	PCIe1.1
Standard in use:	PCIE
Oscilloscope Name:	CBUSSO-NB.lecroy.net Model: SDA13000
Oscilloscope Serial #:	WM000001
Computer:	CBUSSO-NB
Oscilloscope firmware version:	6.5.4.0 (Build 182590)
QualiPHY core version:	5.3.0.6 (Build 105022)
QualiPHY script version:	0.1.2.112
Stylesheet version:	1.2

Summary Table

[Hide Table]

Pass	Test	Measurement	Current Value	Test Criteria
✔		Cables deskew	0	0 +/- 999e-12
✔	1.5	PHY 3.2#1: Mask, non-transition	0	= 0
✔	1.5	PHY 3.2#1: Min V, non-transition	-432.943 mV	-600.000 mV < n < -252.500 mV
✔	1.5	PHY 3.2#1: Max V, non-transition	435.677 mV	252.500 mV < n < 600.000 mV
✔	1.5	PHY 3.2#2: Vtx-diffp-p, transition	0.897456	.8 < n < 1.2
✔	1.5	PHY 3.2#2: Mask, transition	0	= 0
✔	1.5	PHY 3.2#2: Min V, transition	-436.684 mV	-600.000 mV < n < -400.000 mV
✔	1.5	PHY 3.2#2: Max V, transition	448.728 mV	400.000 mV < n < 600.000 mV
✔	1.5	PHY 3.3#1: Mask violations	0	= 0
✔	1.5	PHY 3.3#4: Eye Median to max jitter	39.735 ps	<= 50.000 ps
✔	1.5	PHY 3.3#4: Eye Mean Median to peak jitter	23.771 ps	<= 50.000 ps
✔	1.5	PHY 3.3#4: Eye Min Median to peak jitter	18.732 ps	<= 50.000 ps
✔	1.5	PHY 3.3#9: Minimum Eye Width	346.574 pS	>= 300.000 pS

Details

Deskew Calibration. (Value currently in use: 0)

Pass — Measurement: *Cables deskew*; Limit Name: MinMaxDeskew; Current Value: 0; Test Criteria: 0 +/- 999e-12; Timestamp: 04/02/2008 16:43:20; Description: Check that the deskew between C2 and C3 is coherent. There is no way to check if the current deskew value matches the cable setup. So we check here that the value is inside coherent limits. The deskew calibration is very important. 30 pico seconds could result in wrong results. Deskew value depends on the cables or probe in use, acquisition system and temperatures.

Test 1.5 - Signal Quality.

Pass — Measurement: *PHY.3.2#1: Mask, non-transition*; Limit Name: MaskViolationsTXNonTransition; Current Value: 0; Test Criteria: = 0; Timestamp: 04/02/2008 16:46:19; Description: PHY 3.2#1: Number of mask violations in the non-transition eye at the transmitter package pins

Pass — Measurement: *PHY.3.2#1: Min V, non-transition*; Limit Name: VtxMinNonTransition; Current Value: -432.943 mV; Test Criteria: -600.000 mV < n < -252.500 mV; Timestamp: 04/02/2008 16:46:19; Description: PHY 3.2#1: Minimum voltage in the non-transition eye at the transmitter package pins

Pass — Measurement: *PHY.3.2#1: Max V, non-transition*; Limit Name: VtxMaxNonTransition; Current Value: 435.677 mV; Test Criteria: 252.500 mV < n < 600.000 mV; Timestamp: 04/02/2008 16:46:19; Description: PHY 3.2#1: Maximum voltage in the non-transition eye at the transmitter package pins

Pass — Measurement: *PHY.3.2#2: Vtx-diffp-p, transition*; Limit Name: Vtx-diffp-p; Current Value: 0.897456

Pass — Test Criteria: .8 < n < 1.2; Timestamp: 04/02/2008 16:46:20; Description: PHY 3.2#2: Differential peak to peak voltage measured at the transmitter package pins VDIFFp-p = (2*max(|VD+ - VD-|)) (For a symmetric differential swing.) As defined in the PCI-Express Base Specification, Sec. 4.3.2

Pass — Measurement: *PHY.3.2#2: Mask, transition*; Limit Name: MaskViolationsTXTransition; Current Value: 0; Test Criteria: = 0; Timestamp: 04/02/2008 16:46:20; Description: PHY 3.2#2: Number of mask violations in the transition eye at the transmitter package pins

Pass — Measurement: *PHY.3.2#2: Min V, transition*; Limit Name: VtxMinTransition; Current Value: -436.684 mV; Test Criteria: -600.000 mV < n < -400.000 mV; Timestamp: 04/02/2008 16:46:20; Description: PHY 3.2#2: Minimum voltage in the transition eye at the transmitter package pins

Pass — Measurement: *PHY.3.2#2: Max V, transition*; Limit Name: VtxMaxTransition; Current Value: 448.728 mV; Test Criteria: 400.000 mV < n < 600.000 mV; Timestamp: 04/02/2008 16:46:20; Description: PHY 3.2#2: Maximum voltage in the transition eye at the transmitter package pins

Pass — Measurement: *PHY.3.3#1: Mask violations*; Limit Name: MaskViolationsTXTotal; Current Value: 0; Test Criteria: = 0; Timestamp: 04/02/2008 16:46:20; Description: PHY 3.3#1: Total number of mask violations at the transmitter package pins

Pass — Measurement: *PHY.3.3#4: Eye Median to max jitter*; Limit Name: TtxEyeMedianToMaxJitter; Current Value: 39.735 ps; Test Criteria: <= 50.000 ps; Timestamp: 04/02/2008 16:46:21; Description: PHY 3.3#4: Maximum median to peak jitter seen at the transmitter package pins

Pass — Measurement: *PHY.3.3#4: Eye Mean Median to peak jitter*; Limit Name: TtxEyeMedianToMaxJitter

Pass — Current Value: 23.771 ps; Test Criteria: <= 50.000 ps; Timestamp: 04/02/2008 16:46:21; Description: PHY 3.3#4: Average median to peak jitter seen at the transmitter package pins

Pass — Measurement: *PHY.3.3#4: Eye Min Median to peak jitter*; Limit Name: TtxEyeMedianToMaxJitter; Current Value: 18.732 ps; Test Criteria: <= 50.000 ps; Timestamp: 04/02/2008 16:46:21; Description: PHY 3.3#4: Minimum median to peak jitter seen at the transmitter package pins

Pass — Measurement: *PHY.3.3#9: Minimum Eye Width*; Limit Name: TtxEye; Current Value: 346.574 pS; Test Criteria: >= 300.000 pS; Timestamp: 04/02/2008 16:46:21; Description: PHY 3.3#9: Width of the eye opening at the transmitter package pins

Test 1.5 Signal Quality Eye Diagrams

Timestamp: 04/02/2008 16:46:25

Figure 4. The Test Report includes a summary table with links to the detailed test results

Oscilloscope Option Key Installation

An option key must be purchased to enable the QPHY-PCIe option. Call LeCroy Customer Support to place an order and receive the code.

Enter the key and enable the purchased option as follows:

1. From the oscilloscope menu select **Utilities →Utilities Setup...**
2. Select the **Options** tab and click the **Add Key** button.
3. Enter the **Key Code** using the on-screen keyboard.
4. Restart the oscilloscope to activate the option after installation.

Typical (Recommended) Configuration

QualiPHY software can be executed from the oscilloscope or a host computer. The first step is to install QualiPHY. Please refer to the QualiPHY Operator's Manual for installation instructions.

LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability (Option DMD-1 for oscilloscopes where this is not standard). This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

By default, the oscilloscope appears as a local host when QualiPHY is executed in the oscilloscope. Follow the steps under **Oscilloscope Selection** (as follows) and check that the IP address is 127.0.0.1.

Remote (Network) Configuration

It is also possible to install and run QualiPHY on a host computer, controlling the oscilloscope with a Network/LAN Connection.

The oscilloscope must already be configured, and an IP address (fixed or network-assigned) must already be established.

Oscilloscope Selection

Set up the oscilloscope using QualiPHY over a LAN (Local Area Network) by doing the following:

1. Make sure the host computer is connected to the same LAN as the oscilloscope. If unsure, contact your system administrator.
2. From the oscilloscope menu, select **Utilities → Utilities Setup…**
3. Select the **Remote** tab.
4. Verify the oscilloscope has an IP address and the control is set to TCP/IP.
5. Run QualiPHY in the host computer and click the **General Setup** button.
6. Select the **Connection** tab.
7. Enter the IP address from step 4 (previous).
8. Click the **Close** button.

QualiPHY is now ready to control the oscilloscope.

QualiPHY tests the oscilloscope connection after clicking the **Start** button. The system prompts you if there is a connection problem. QualiPHY's **Scope Selector** function can also be used to verify the connection. Please refer to the **QualiPHY Operator's Manual** for explanations on how to use Scope Selector and other QualiPHY functions.

Accessing the QPHY-PCIe Software using QualiPHY

This topic provides a basic overview of QualiPHY's capabilities. Please refer to the **QualiPHY Operator's Manual** for detailed information.

Access the QPHY-PCIe software using the following steps:

1. Wait for the oscilloscope to start and have its main application running.
2. Launch QualiPHY from the **Analysis** menu if installed on the oscilloscope or from the desktop icon if installed on a host computer.
3. From the QualiPHY main window (as follows), select **Standard**, then **PCIE** from the pop-up menu (if not already selected). If you check the **Pause on Failure** box (circled) QualiPHY prompts to retry the measure whenever a test fails.

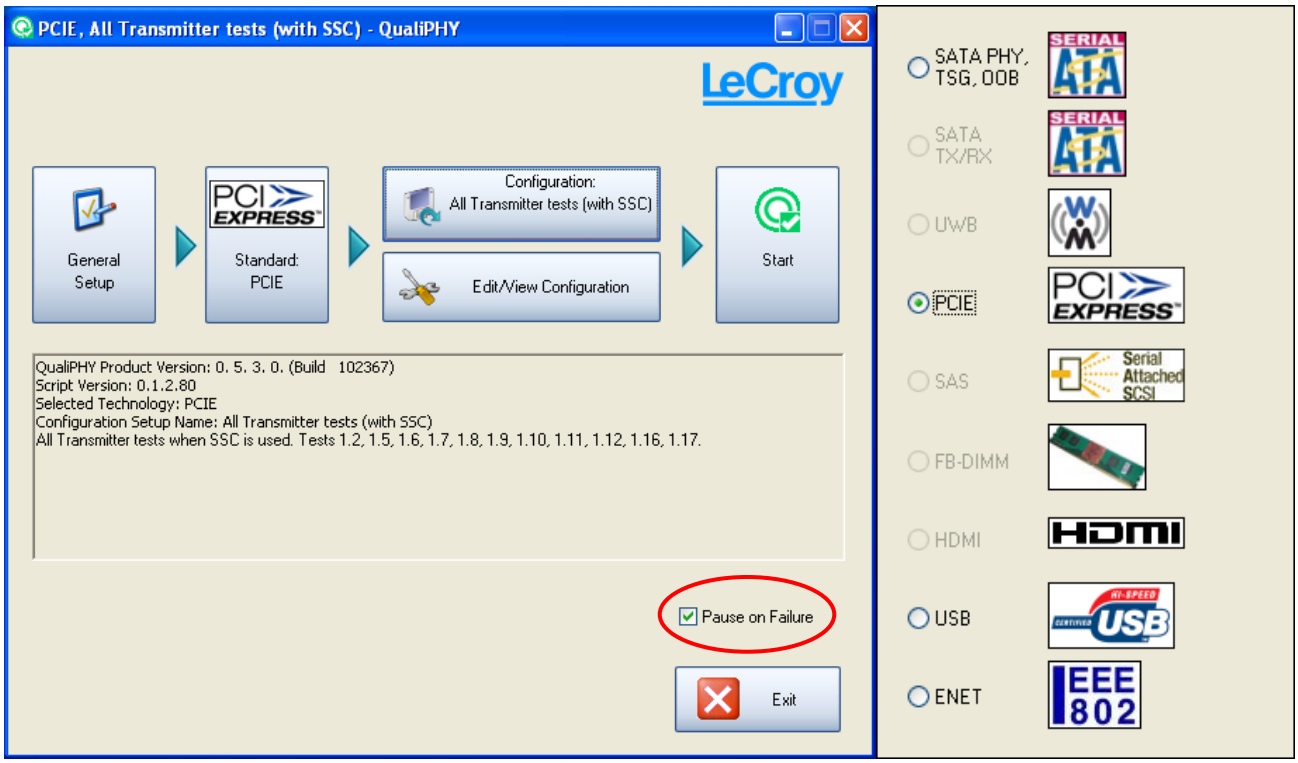


Figure 5. QualiPHY main menu and compliance test Standard selection menu

4. Click the **Configuration** button in the QualiPHY main menu:

5. Select a configuration from the pop-up menu:

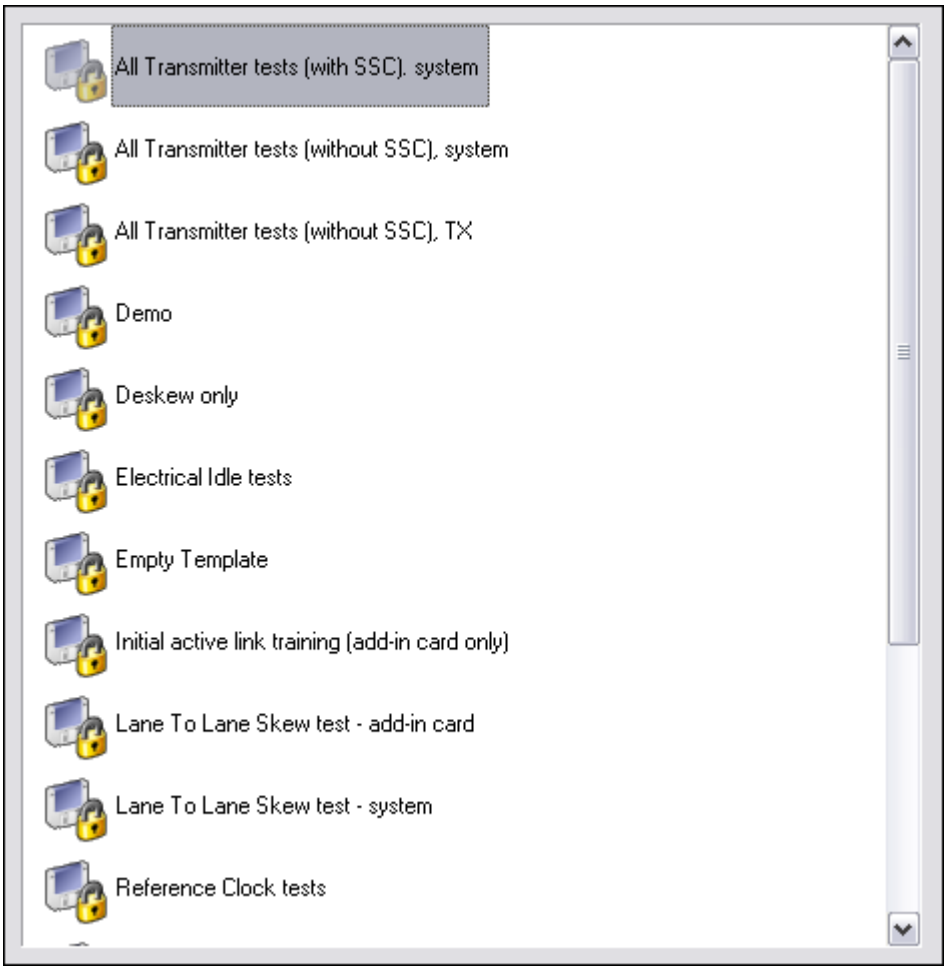


Figure 6. QualiPHY configuration selection menu

6. Click **Start**.

7. Follow the pop-up window prompts.

Customizing QualiPHY

The predefined configurations in the **Configuration** screen cannot be modified. However, you can create your own test configurations by copying one of the standard test configurations and making modifications. A description of the test is also shown in the description field when selected.

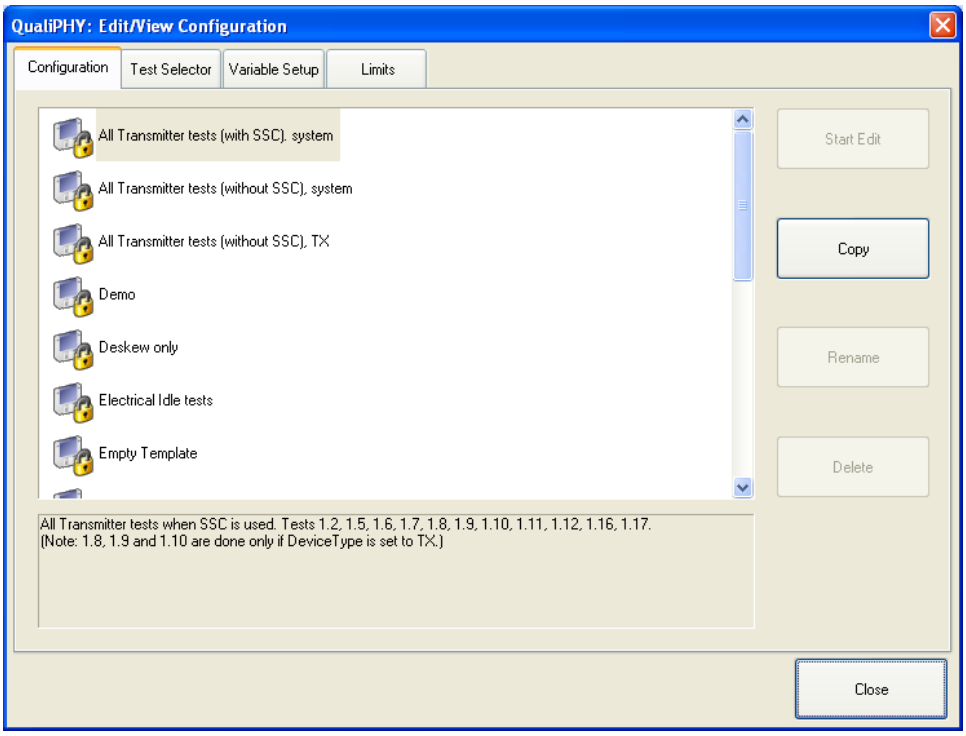


Figure 7. QualiPHY test item selection menu

Once a custom configuration is defined, script variables and the test limits can be changed by using the **Variable Setup** and **Limits Manager** from the **Edit/View Configuration** window.

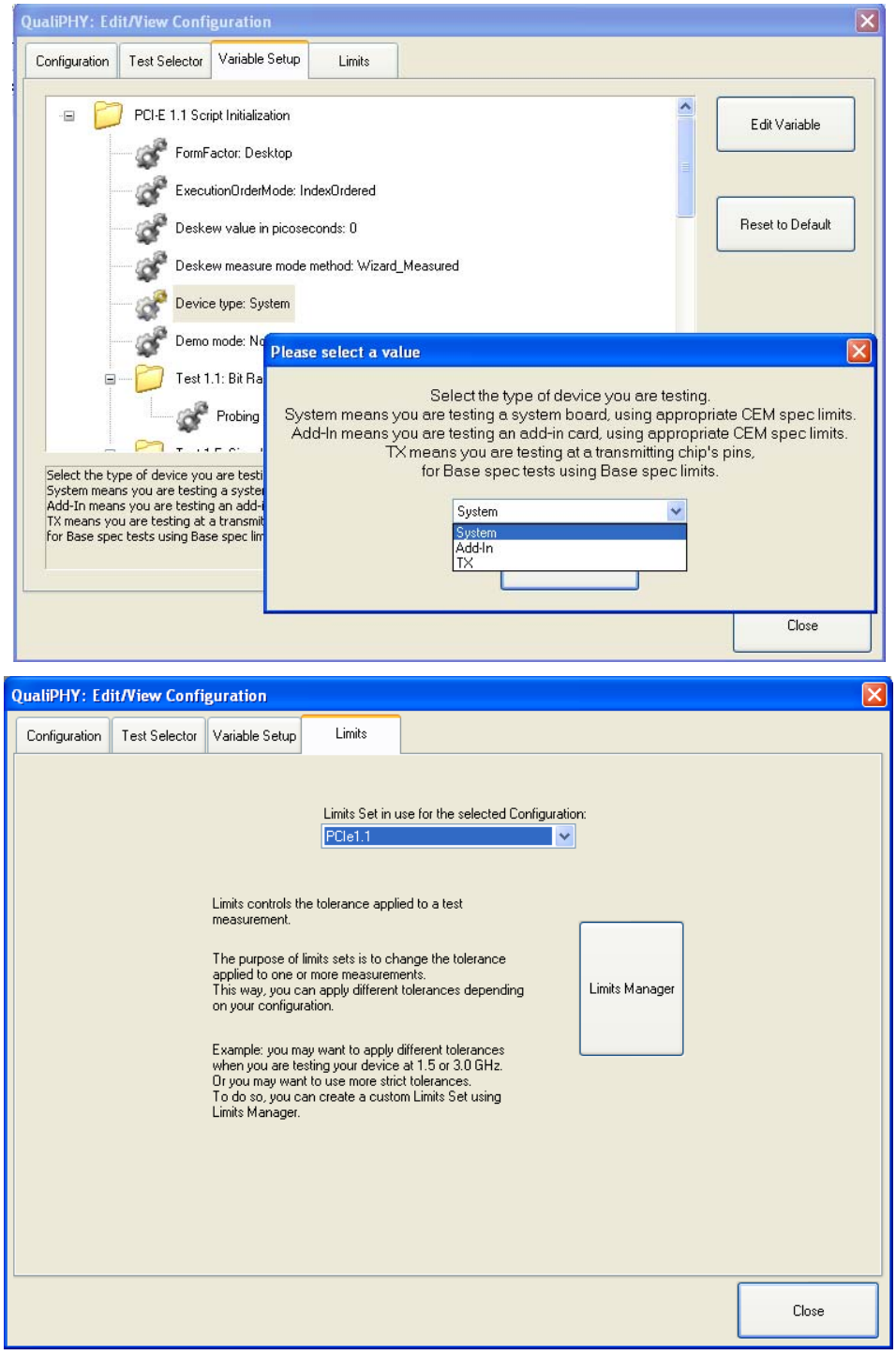


Figure 8. Variable Setup and Limits Manager windows

QPHY-PCIe Operation

After pressing **Start** in the QualiPHY menu, the software instructs how to set up the test using pop-up connection diagrams and dialog boxes.

Figure 9. Start button

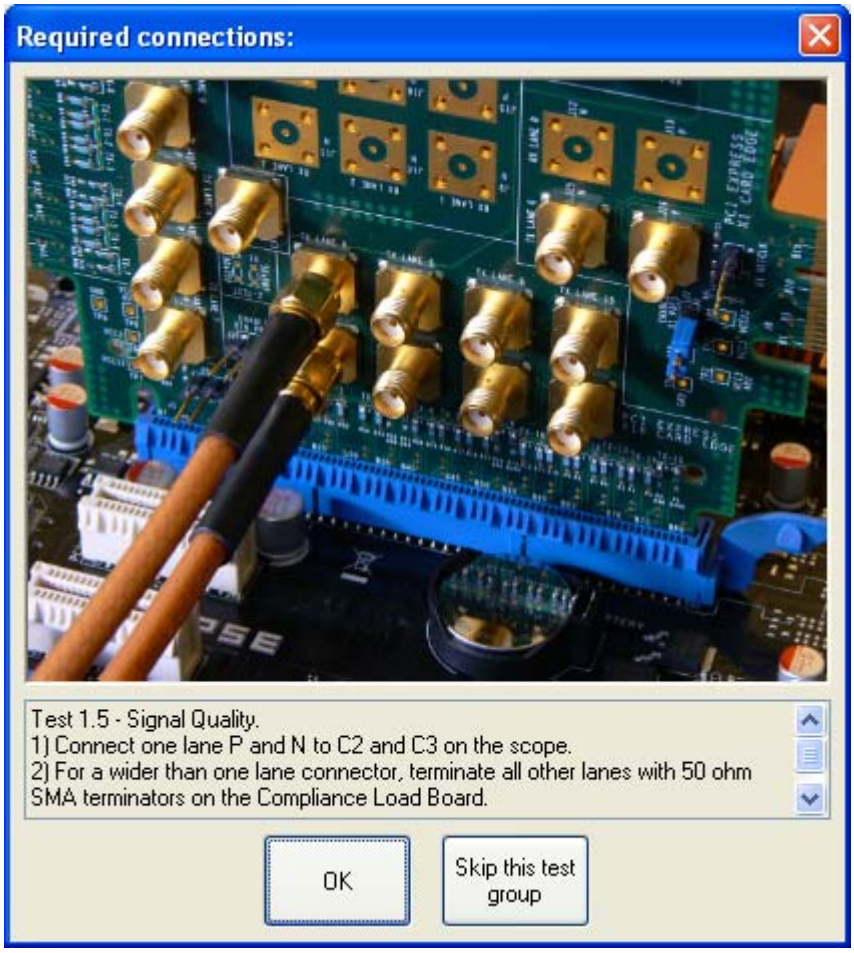


Figure 10. Example of pop-up connection diagram and dialog box

INTRODUCTION TO PCI-EXPRESS

PCI Express is a serial version of the commonly used PCI bus designed for PC's and servers. This serial interface adds scalability through the use of multiple lanes, and flexibility through such features as switching. PCI Express is a multi-lane interface that operates at a signaling rate of 2.5 Gb/s on each lane. The differential signal contains both normal and inverted signal lines designated D^+ and D^-, and the signaling voltages are nominally 800 mV peak-to-peak.

PCI Express is designed to operate on standard PC motherboards using low-cost PCI-type sockets. This implies several things about the signal characteristics. First, spread spectrum clocking must be supported to control emissions in desktop applications. Second, because standard PC motherboards must be used, the signal is pre-emphasized to control inter-symbol interference. Finally, many implementations of serial data receivers employ an "over sampling" mode that takes many samples per bit to find the data transitions rather than using a recovered clock for this purpose.

PCI Express Device Development Process

With the introduction of PCI Express Gen2 in Spring 2005, High Speed PCI Express has arrived. As a result, PCI Express standards have evolved to allow existing Gen1 (2.5 Gb/s) designs to interact with the new, demanding 5 Gb/s requirements. New requirements for PCI Express Gen1 were incorporated into the PCIE Version 1.1 specification, effective April 2005. PCI-SIG encourages new and experienced electrical interface designers to undertake new designs using a *Predictable Path to Design Compliance*.

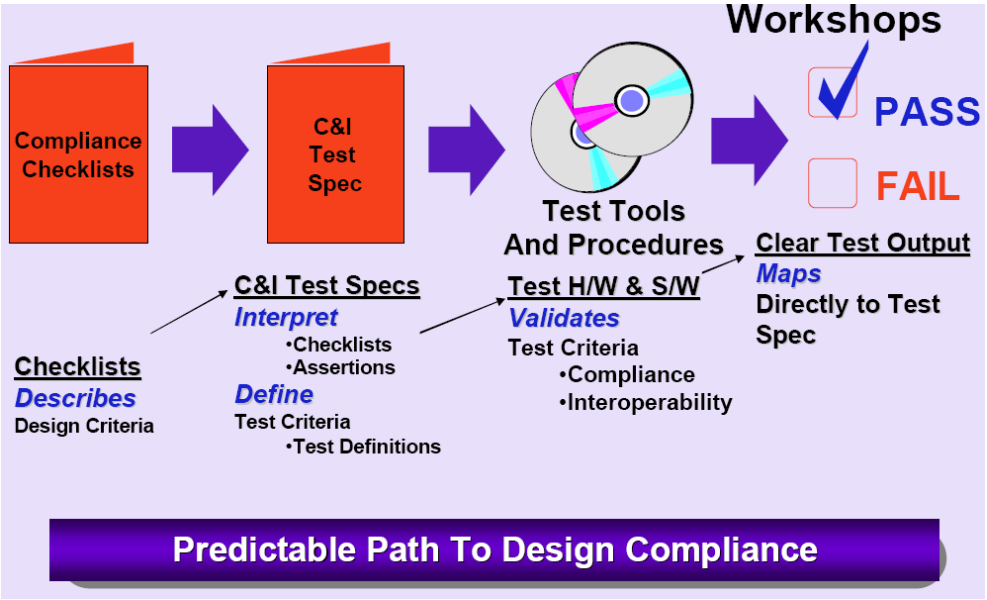


Figure 11. PCI Express path to design compliance

Note: The previous image is slide 40 from the presentation *PCIe 1.1 Training Day 12.06.04 – updated.pdf*, presented at a PCI-SIG workshop by the consortium.

PCI Express Device Development Process and Compliance Tests

The PCI Express **Compliance** test requirements are derived from the test specification document, which is interpreted from the design checklist. The design checklist is a set of requirements that must all be met during the design phase of a PCI Express-compliant device. An example of a few requirements from the design checklist is shown as follows:

PHY.2.6#1	Training sequence ordered-sets are never scrambled but always 8b/10b encoded.	yes ___ no___
PHY.3.1#25	The receiver terminations must remain enabled in Electrical Idle.	yes ___ no___
PHY.3.2#5	The Beacon signal must contain minimum width pulses >= 2 ns.	yes ___ no___

Figure 12. Example requirements from the PCI Express design checklist

The test specification / Electrical Design Considerations contain a list of **Assertions** that are derived from the checklist. For example, the symbol rate must be 2.5 Gb/s +/-300 ppm. Each assertion has a specific measurement that is used to verify it, the **Test Number**. While there are many tests in the specification, only the signal quality test is performed for **Compliance**.

The new LeCroy PCI Express software supports the measurement of PCI Express signals in two modes of operation:

- ***Compliance Test Mode***, or signal quality test, based on Intel's SIGTEST dynamically linked library (dll) and used for test and evaluation at PCI-SIG sponsored electrical test workshops. These tests are covered in the Electrical Design Considerations document under Tests 1.4 and 1.5, and can be accessed by manual control on the DSO or by selecting the corresponding tests under QualiPHY.
- ***Checklist Test Mode or Designers Checklist Mode***. In this case, the QualiPHY script provides capabilities to run all the test steps required or some group of tests, as many times as specified, and in accordance with the device type (Add-In card, System card, or TX) supported by the device under development. For example, a developer may only be interested in the TX performance of the chipset, and then only the Transmitter Tests are selected for verification.

PCI EXPRESS MEASUREMENT THEORY

Eye Pattern and Jitter Measurements

PCI Express signal quality tests are performed using eye pattern analysis. The eye pattern allows measurement of voltage and jitter. The measurement methodology that has been adopted for eye patterns in this standard is designed to accommodate the requirements of over-sampling detectors and spread spectrum clocking. The method relies on the acquisition of consecutive unit intervals of the data stream sampled at a minimum rate of 20 GS/s.

Version 1.1 Measurements

The revised version of the specification places a premium on the acquisition record size requirements: 1 million UI, which translates to 8 Mpts acquisition record size when running at 20 GS/s. The reference clock is assumed to have been cleaned and therefore contributes zero jitter as follows:

> *The TTX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget using the clock recovery function specified in Section 4.3.3.2 of the PCI Express Base Specification. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal, as opposed to the averaged time value. This parameter is measured with the equivalent of a zero-jitter reference clock. The TTX-EYE measurement is to be met at the target bit error rate. The TTX-EYE-MEDIAN-to-MAX-JITTER is to be met using the compliance pattern at a sample size of 1,000,000 UI.*

The new clock recovery applies a first order high-pass filter with a -3 dB cutoff frequency of 1.5 MHz, rolling off at a rate of -20 dB/decade.

Note: In addition, the new clock recovery function will apply to devices (for example, Add-in cards) that rely on a clean clock. For System board designers, however, the burden of proving that the reference clock is a clean clock is a NEW requirement for PCIE Version 1.1 compliant designs.

PCI EXPRESS MEASUREMENT PREPARATION

Before beginning any test or data acquisition, the oscilloscope must be warmed for at least 20 minutes. Calibration is automatic under software control and no manual calibration is required. The following procedure explains how to compensate for the skew of the cables.

This procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

Note: This procedure describes how to manually deskew cables. The QPHY-PCIe script will automate this entire process.

Channel Deskew using Oscilloscope Calibrator Output (SMA Cables)

PCI Express signals are properly probed using two separate channels on the oscilloscope connected to the appropriate SMA jacks on the test fixture. The highest measurement accuracy is achieved when the timing skew between the two channels is calibrated. This is performed using the **Deskew** control on one of the two channels to which the differential signal is connected, as follows:

1. Attach the calibrator signal to both input channels using a T connector or resistive divider to route the calibrator signal on the SDA front panel through the same cables that will be connected to the fixture. The calibrator peak voltage should be set to the same value as the nominal voltage of D^+ and D^-.

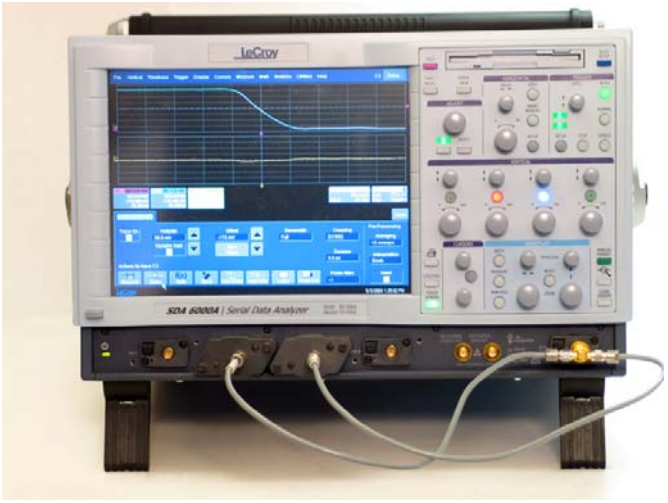


Figure 13. Deskew cable setup

2. Set interpolation of both channels to **Sin(x)/x**, using the **Interpolation** control in the **Vertical Adjust** dialog for each channel.
3. Check the **Invert** checkbox on one channel.

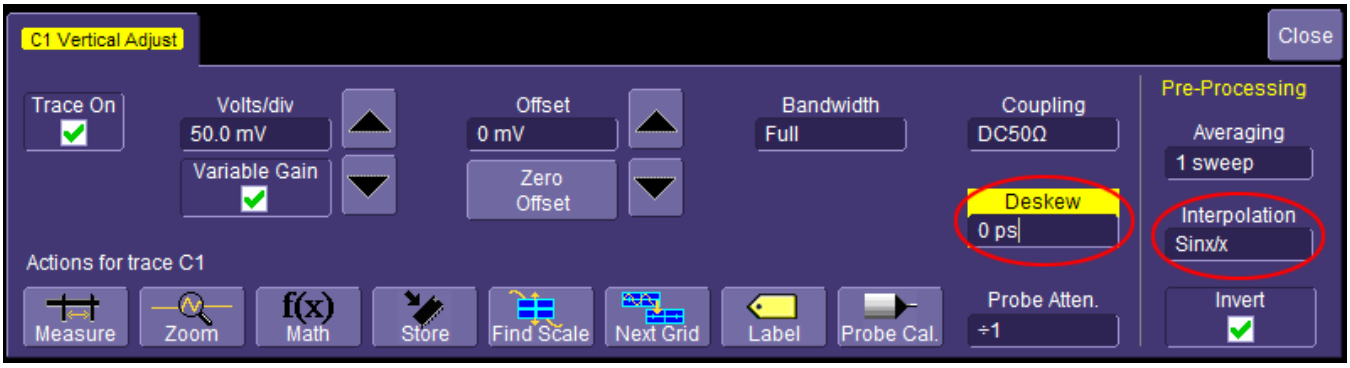


Figure 14. Deskew control in channel menu: adjust this value to achieve minimum skew

4. Create a Difference math waveform by selecting **Math → Math Setup…** from the menu bar.

   Touch the **Operator1** field and select **Difference** from the **Select Math Operator** menu.

   Enter the channels to which your signal is connected in the **Source1** and **Source2** fields. The math function is thus defined as the difference between the 2 channels probing the D^+ and D^- signals.

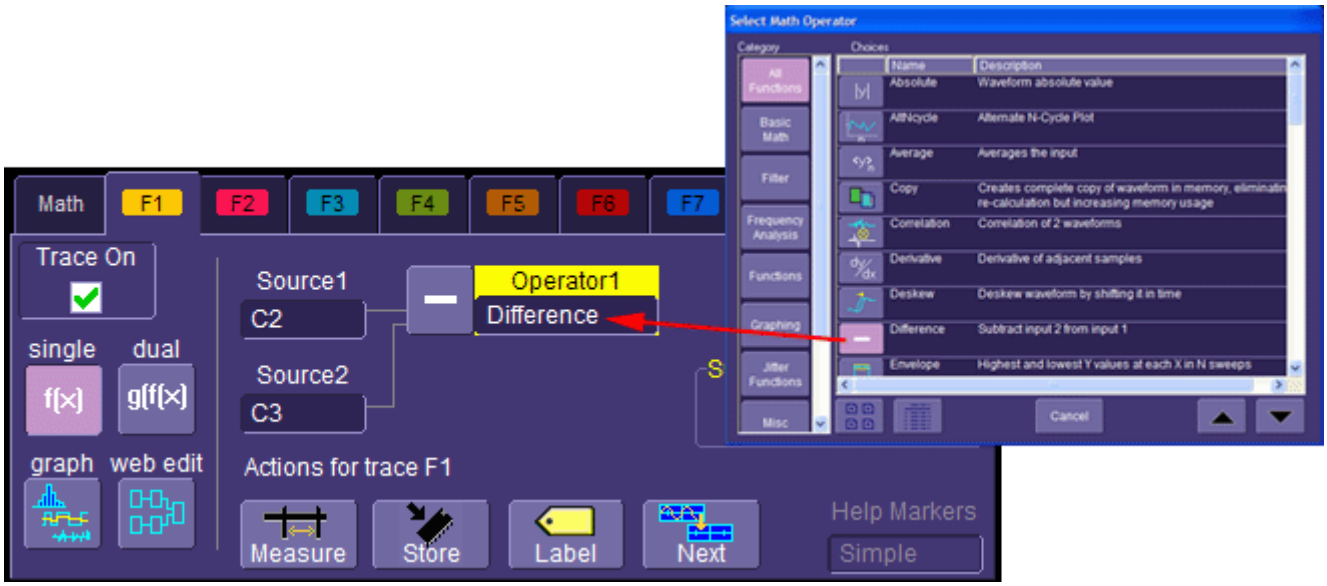


Figure 15. Math setup

5. While viewing the math trace, adjust the **Deskew** control in one of the channels until the math trace is as flat as possible.

Note: With the **Deskew** control highlighted, you can use the front panel adjust knob to make the adjustment.

The best accuracy is achieved by setting the level of the calibrator signal to match the expected levels of the signal under test, and with the calibrator set to its maximum frequency (5 MHz). The calibrator settings can be found in **Utilities → Aux Output**.

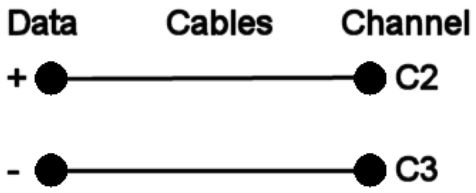
Channel Deskew using Device Under Test Signal (SMA Cables)

This is a multi-step procedure which is more complicated than the procedure given above. Its advantages are:

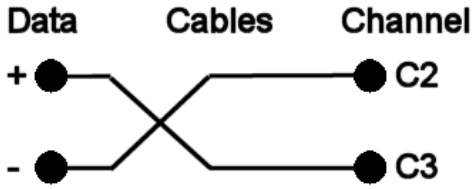
- No adapters needed.
- De-skew at the same V/div settings you'll use to capture your data (because you are capturing your data for this procedure)
- If the differential data signal has higher speed edges than the oscilloscope's AUX OUT, it is easier to get good timing measurements with the faster edges. This is definitely the case for PCI-Express.

Here is the step by step procedure:

1. Connect a differential data signal to C2 and C3 using two approximately matching cables. Set up the oscilloscope as you plan to use it. Set the timebase to capture a few repetitions of the compliance test pattern (at least a few dozen edges). Press **Auto**, so the oscilloscope acquires.



2. On the C3 menu, check **Invert**. Now C2 and C3 should look the same.
3. Using the **Measure Setup**, set P1 to measure the Skew of C2, C3. Turn on **Statistics** (**Measure** menu). Write down the mean skew value after it stabilizes. This mean skew value is the addition of Data skew + cable skew + channel skew.
4. Swap the cable connections on the Data source side (on the test fixture), and then press the **Clear Sweeps** button on the oscilloscope (to clear the accumulated statistics; since we changed the input).



5. Write down the mean skew value after it stabilizes. This mean skew value is the addition of (-Data skew) + cable skew + channel skew.
6. Add the two mean skew values and divide the sum in half:

$$\frac{[\text{Data skew} + \text{cable skew} + \text{channel skew}] + [(-\text{Data skew}) + \text{cable skew} + \text{channel skew}]}{2}$$

7. The above formula simplifies to:

$$[\text{cable skew} + \text{channel skew}]$$

8. Set the resulting value as the **Deskew** value in C2 menu.
9. Restore the cable connections to their Step 1 settings (previous). Press the **Clear Sweeps** button on the oscilloscope. The mean skew value should be approximately zero - that is the data skew. Typically, results are <1ps given a test fixture meant to minimize skew on the differential pair.

10. On the C3 menu, un-check the **Invert** checkbox and turn off the parameters.

Now the oscilloscope inter-channel skew and cable skew is compensated for, you are ready to test.

The procedure as given above relies on the default setup of the Skew parameter (which is: detecting positive edges on both signals, at 50%). C3 was inverted in order to make C2 and C3 both have positive edges at the same time. The default setup of any parameter is in effect at the time it is set up.

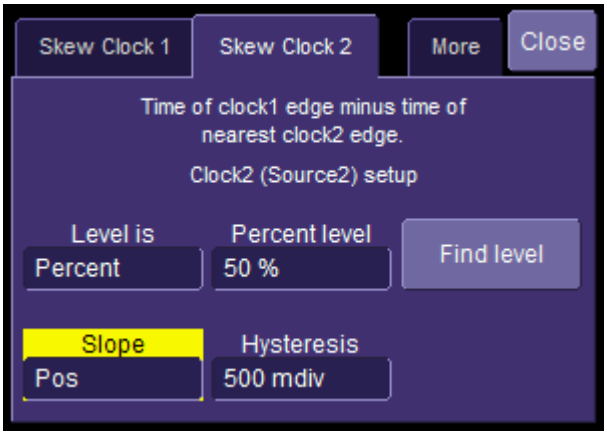


Figure 16. The Skew parameter right side dialog, Skew clock 2 tab, showing default setup

Differential Probe Calibration

The PCI Express signal can be applied to a single channel of the SDA using a differential probe, or directly to two channels using one of the test fixtures described above. All tests in the script can be done using 2 single ended connections. Directly cabling the signals to the scope is the recommended configuration. In either case, the signal level should be maximized on the instrument to achieve the best overall accuracy. The signal level is set in the **Vertical Adjust** dialog, or by using the front panel knobs. The best peaking can be achieved by checking the **Variable Gain** checkbox, which allows finer gain steps in the control knobs.

Note: The script automatically determines the optimal gain setting for running the test. This information is provided in order to help perform the tests manually if required.

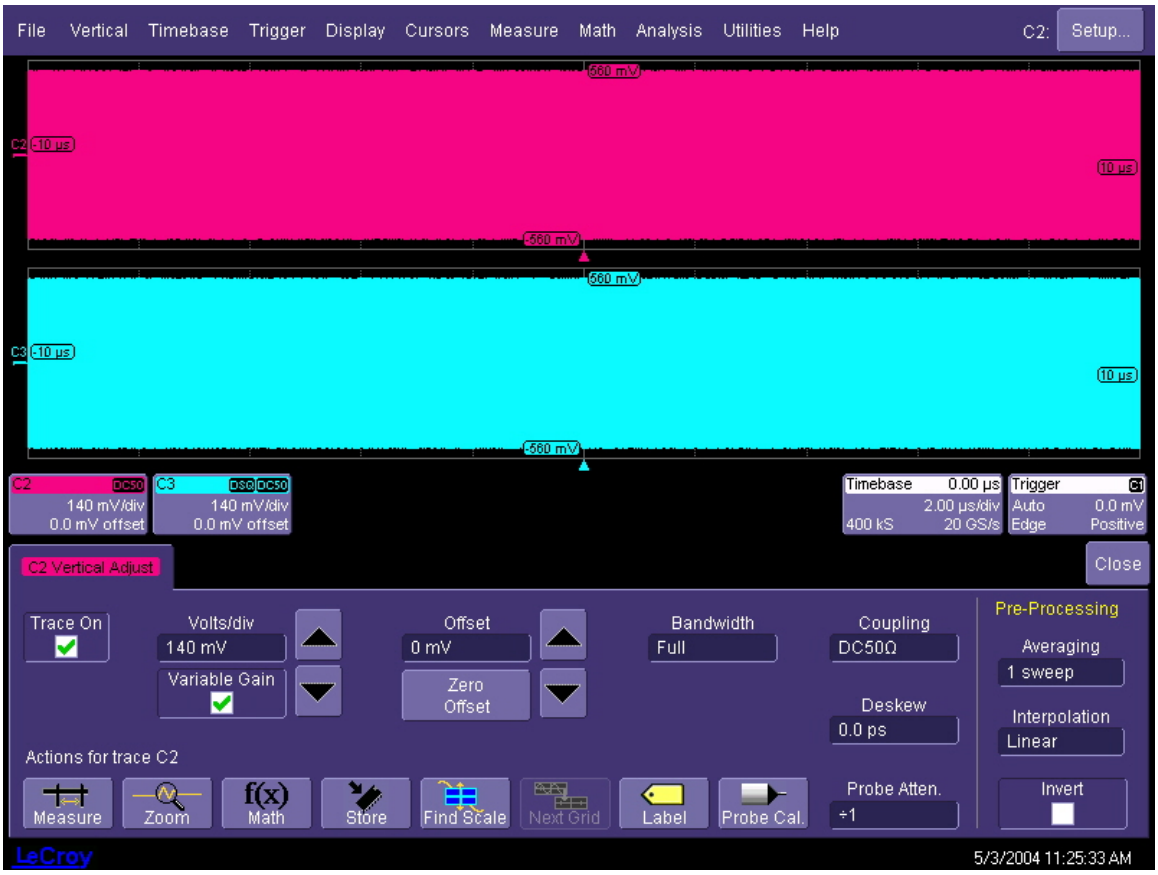


Figure 17. Signals properly adjusted for best accuracy

Note: The signal levels should be adjusted in the Vertical Adjust dialog so at least 6 vertical divisions are filled.

For SDA 6000A

The horizontal scale should be set to a fixed sampling rate of 20 GS/s. This requires that **Auto** or **2** channels be selected in the **Active Channels** control in the **Horizontal** (Timebase) dialog. The record length should be set to a minimum of **8 MS** using the **Time/Division** control or the front panel horizontal scale knob. Longer records give more accurate results but also take more time to compute.

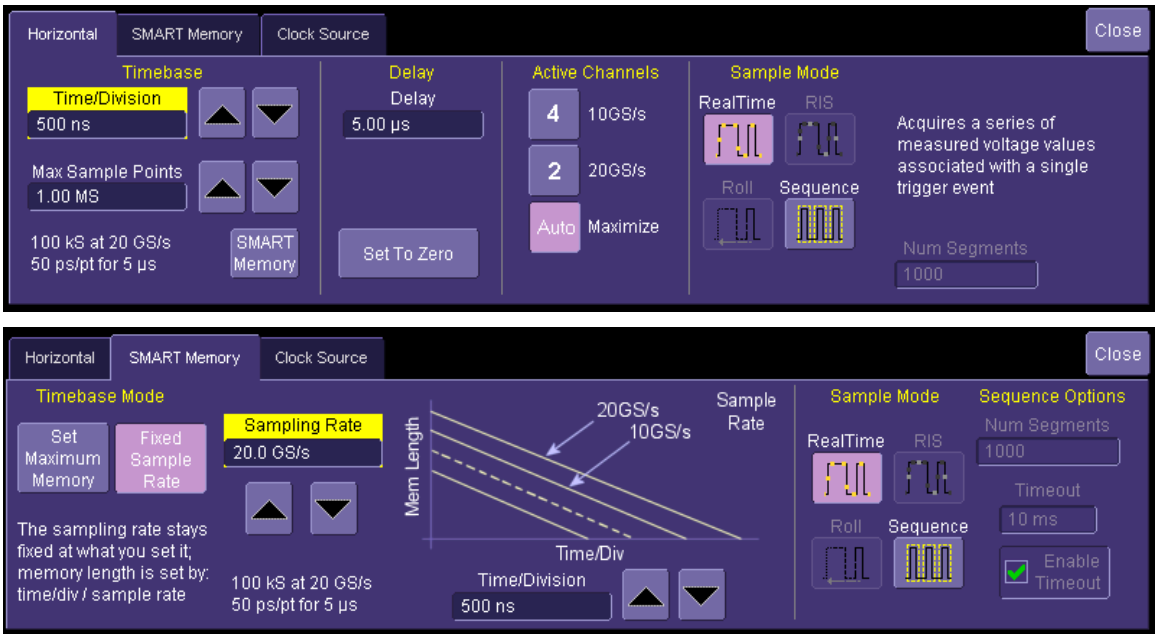


Figure 18. Horizontal and memory setup menus properly configured for testing PCI Express signals

Note: The maximum (20 GS/s) sampling rate must be used. The SDA6020 model does not have the Active Channels control since all channels sample at 20 GS/s.

The signal under test is selected from the **Data Source** menu in the **Serial Data Analysis** main dialog. The source can be any channel, memory, or math trace.

Note:

- If a differential probe is being used to couple the signal to the instrument, the channel to which the probe is attached should be entered into the **Data Source** control.
- When probing with 2 channels of the instrument attached to a compliance test fixture, a math trace should be defined as the difference between the channel connected to the D^+ and the channel connected to the D^- lines on the fixture. The channels should be deskewed as previously described.
- It is also possible to perform measurements on waveform files stored in memory. Either on the system hard disk or in non-volatile memory. Subtract the memory traces if they are stored as separate (+ and -) waveforms, as previously described, or enter the memory into the **Data Source** control directly.

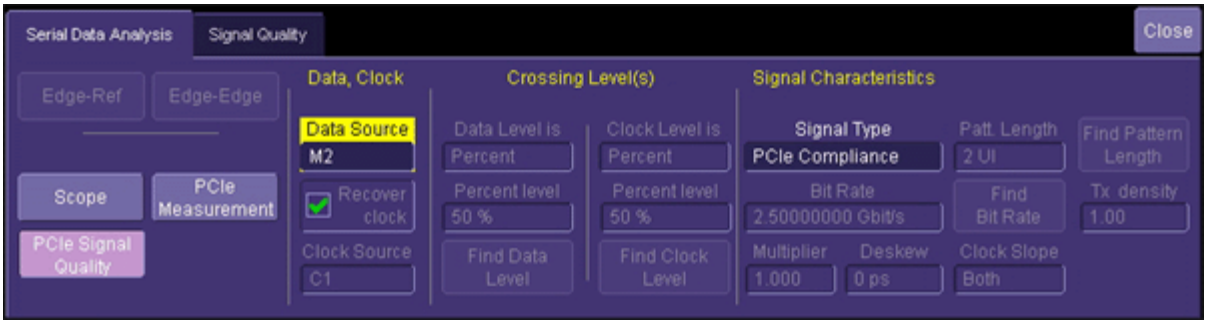


Figure 19. Selecting signal under test in Serial Data Analysis dialog

QPHY-PCIe TEST CONFIGURATIONS

Configurations include variable settings and limit sets as well, not just test selections. See the QPHY-PCIe Variables section for a description of each variable value and its default value. There is only one limit sets for QPHY-PCIe (PCIe1.1).

All Transmitter tests (with SSC) - system

This configuration performs all of the necessary tests for a transmitter with SSC. The limit set in use is PCIe1.1. All of the variables are set to their default settings. Please note that **CleanClock** is set to **No** (in Test 1.5 and Test 1.16) in this configuration. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.2 SSC TX Data and Modulation Rate
- Test 1.5 Signal Quality
- Test 1.6 TX DC Common Mode Voltage
- Test 1.7 TX L0 to Electrical Idle to L0
- Test 1.8 RX Detect Voltage
- Test 1.9 RX Detect Hi-Z
- Test 1.10 TX Detect Low-Z
- Test 1.11 Lane-to-Lane Skew
- Test 1.12 TX Output Rise/Fall
- Test 1.16 TX Transitions from Electrical Idle
- Test 1.17 Receiver Detection Sequence

All Transmitter tests (without SSC) - system

This configuration performs all of the necessary tests for a transmitter without SSC. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.4 Non-SSC TX Data Rate
- Test 1.5 Signal Quality
- Test 1.6 TX DC Common Mode Voltage
- Test 1.7 TX L0 to Electrical Idle to L0
- Test 1.8 RX Detect Voltage
- Test 1.9 RX Detect Hi-Z
- Test 1.10 TX Detect Low-Z
- Test 1.11 Lane-to-Lane Skew
- Test 1.12 TX Output Rise/Fall
- Test 1.16 TX Transitions from Electrical Idle
- Test 1.17 Receiver Detection Sequence

All Transmitter tests (without SSC) - TX

This configuration performs all of the necessary tests for a transmitter without SSC. The limit set in use is PCIe1.1. All of the variables are set to their default settings except **Device type** is set to **TX**. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.4 Non-SSC TX Data Rate
- Test 1.5 Signal Quality
- Test 1.6 TX DC Common Mode Voltage
- Test 1.7 TX L0 to Electrical Idle to L0
- Test 1.8 RX Detect Voltage
- Test 1.9 RX Detect Hi-Z
- Test 1.10 TX Detect Low-Z
- Test 1.11 Lane-to-Lane Skew
- Test 1.12 TX Output Rise/Fall
- Test 1.16 TX Transitions from Electrical Idle
- Test 1.17 Receiver Detection Sequence

Demo

This configuration performs tests on saved waveforms found in the D:\Waveforms\PCIe\Demo directory. All of the variables are set to their default settings except **Deskew measure mode method** is set to **User_Defined** and **DemoMode** is set to **Yes**. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.2 SSC TX Data and Modulation Rate
- Test 1.5 Signal Quality
- Test 1.12 TX Output Rise/Fall

The Demo configuration is meant for demonstration purposes. It uses waveforms in folder D:\Waveforms\PCIe\Demo\ on the scope, the waveform names are pcie_with_sscp.trc and pcie_with_sscm.trc. Waveforms of those names in that folder are recalled into Memories and tested. Connection diagrams are not shown in demo mode.

Deskew only

This configuration performs only the Deskew procedure. After you perform the Deskew procedure, you can copy the configuration you want to use, set the **Deskew value in picoseconds** variable, and set the **Deskew measure mode method** variable to **User_defined**. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization

Electrical Idle tests

This configuration looks for COM-IDL-IDL-IDL before dropping into Electrical Idle in Test 1.7; it makes electrical measurements on the signal while in Electrical Idle (also in Test 1.7), and it tests that the transmitted signal meets all compliance requirements at the required time after exiting Electrical Idle in Test 1.16. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.7 TX L0 to Electrical Idle to L0
- Test 1.16 TX Transitions from Electrical Idle

Empty Template

This configuration is intentionally left blank so it can easily be copied and configured to the user's custom configuration. The limit set in use is PCIe1.1. All of the variables are set to their default settings.

- PCI-E 1.1 Script Initialization is selected as it is required prior to any test.

Initial active link training (add-in card only)

This configuration measures the time from PERST de-assertion to link active (L0). The limit set in use is PCIe1.1. All of the variables are set to their default settings except **Device type** is set to **Add-In**. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.18 Initial Active-Link Training

Lane To Lane Skew test - add-in card

This configuration performs only the Lane-to-Lane skew test for an add-in card. The limit set in use is PCIe1.1. All of the variables are set to their default settings except **Device type** is set to **Add-In**. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.11 Lane-to-Lane Skew

Lane To Lane Skew test - system

This configuration performs only the Lane-to-Lane skew test for a system. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.11 Lane-to-Lane Skew

Reference Clock tests

This configuration performs only the Reference Clock Tests. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.19 Reference Clock Tests

Secondary clock domain test

This configuration performs only the Bit Rate Clock Accuracy tests. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.1 Bit Rate Clock Accuracy

Signal Quality Test - TX

This configuration performs only the Signal Quality tests for a transmitter. The limit set in use is PCIe1.1. All of the variables are set to their default settings except **Device type** is set to **TX**. Please note that **CleanClock** is set to **No** for test 1.5. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.5 Signal Quality

Signal Quality Test (CEM) - add-in card

This configuration performs only the Signal Quality tests as specified in the CEM specification for an add-in card. The limit set in use is PCIe1.1. All of the variables are set to their default settings except **Device type** is set to **Add-In** and **CleanClock** is set to **Yes** for test 1.5. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.5 Signal Quality

Signal Quality Test (CEM) - system (with SSC)

This configuration performs only the Signal Quality tests as specified in the CEM specification for a system. The limit set in use is PCIe1.1. All of the variables are set to their default settings. Please note that **CleanClock** is set to **No** for this configuration. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.5 Signal Quality

SSC Data and Modulation Rate test

This configuration performs only the SSC TX Data and Modulation Rate tests. The limit set in use is PCIe1.1. All of the variables are set to their default settings. The tests that are performed are:

- PCI-E 1.1 Script Initialization
- Test 1.2 SSC TX Data and Modulation Rate

QPHY-PCIe VARIABLES

FormFactor

Used to select whether the Device Under Test is a PCI Express **Desktop** or **Mobile** device**.** The default for this variable is **Desktop**.

ExecutionOrderMode

Allows a choice between the order of the script (index order) and another order meant to minimize cable changes if some of the tests will be done with a diff probe. The default for this variable is **IndexOrdered**. The other option is **CablingOrdered**.

Deskew value in picoseconds

Used to entered a default deskew value. The default for this variable is **0**.

Deskew measure mode method

Used to select between entering their own deskew value or running the deskew wizard. The default for this variable is **Wizard_Measured**. The other option is **User_Defined**.

Device type

Used to select whether the Device Under Test is a PCI Express **System** or **Add-In** Card or **TX**. Measurements on Systems use a CLB; measurements on Add-In cards use a CBB; and measurements on a TX are made at the pins of the transmitting chip. If this value is set incorrectly, it will result in the wrong connection diagrams being displayed. The default for this variable is **System**.

DemoMode

This option is used to put the script into demo mode. When in this mode the script will run on saved waveforms that are placed in the D:\waveforms\PCIe\Demo directory on the oscilloscope. The default for this variable is **No**. This variable is set to **Yes** only in the Demo configuration.

Test 1.1 Bit Rate Clock Accuracy Variables

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.1. The default for this variable is **Single-Ended**.

Test 1.5: Signal Quality

CleanClock

Used to specify if revision 1.1 of the CBB is being used for Add-In card test. Revision 1.1 of the CBB has a clean clock source. The default for this variable is **No**.

Test 1.7 TX L0 to Electrical Idle to L0 Variables

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.7. The default for this variable is **Single Ended**.

Test 1.9 RX Detect Hi-Z

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.9. The default for this variable is **Single Ended**.

Test 1.10 RX Detect Low-Z

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.10. The default for this variable is **Single Ended**.

Test 1.12 TX Output Rise/Fall

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.12. The default for this variable is **Single Ended**.

Test 1.16 TX Transitions from Electrical Idle Variables

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.16. The default for this variable is **Single-Ended**.

CleanClock

Used to specify if revision 1.1 of the CBB is being used for Add-In card test. Revision 1.1 of the CBB has a clean clock source. The default for this variable is **No**.

Test 1.18 Initial Active Link Training

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.18. The default for this variable is **Single-Ended**.

Reference Clock Differential Tests

Probing method

Used to select either a **Differential** Probe or **Single-Ended** measurement for Test 1.19. The default for this variable is **Single-Ended**.

Period: SSC

Used to select if the device clock has SSC turn on. The default for this variable is **No**.

QPHY-PCIe LIMIT SETS

PCIe1.1

Contains all limits are given in PCIe specification revision 1.1.

QPHY-PCIe TESTS

PCIe 1.1 Script Initialization

Test 1.1: Bit Rate Clock Accuracy

Assertion: PHY.3.1#1

Purpose: Test Bit Rate Clock Accuracy, and matching of two clock domains (not sharing a reference clock)

Description: This test is only necessary when one side of a link does not directly use the root clock. In this case the device's secondary clock domain must track and replicate the root clock domain (including SSC if applicable). This test requires connection to the clock of the transmitter and the clock of the receiver. This test verifies that the bit rate clocks for the transmitter and receiver of each link are within 600 ppm of each other at all times in both SSC and non-SSC modes. It uses the SDA to capture outputs from both clocks simultaneously and uses software within the SDA to calculate and compare the frequency of each clock at any given time in the sample.

Note: Bit rate without SSC and SSC modulation limits and frequency are tested in Test 1.2 and Test 1.4, as follows.

Test 1.2: SSC TX Data and Modulation Rate

Assertions: PHY.3.1#2, PHY.3.1#3

Purpose: Test SSC TX Data and Modulation Rate

Method:

1. Place transmitter under test in compliance pattern mode.
2. The SDA captures more than 10 cycles of SSC (more than the required 30.3us of continuous data).
3. The SDA displays a track of bit rate vs. time computed from the waveform data, filtered as required. Data rate limits SSC modulation rate are computed.

Test 1.4: Non-SSC TX Data Rate

Assertions: PHY.3.3#2

Purpose:

Method:

1. Place transmitter under test in compliance pattern mode.

2. The SDA acquires multiple sweeps of data of sufficient length to measure the Bit Rate (the data rate) with accuracy several times better than the required limits even if the signal has maximum allowed jitter, and computes the data rate from each sweep.

3. The maximum and minimum data rate values computed in step 2 are tested to be within 300ppm of nominal.

Test 1.5: Signal Quality

Assertions: PHY.3.2#1, PHY.3.2#2, PHY.3.2#14, PHY.3.3#1, PHY.3.3#4, PHY.3.3#9

Purpose:

The PCI-Express Base Specification, Rev 1.1 requires that jitter measurements be met with a sample size of 1 million UI. This test uses a 200 µs (500k UI) acquisition; therefore, for compliance this test should be run twice.

1. For TX: Attach the Compliance Test Load on all the transmitter data lines for the DUT. For System: Insert the CLB. For Add-in cards: Insert the card into the CBB.
2. Place the transmitter in compliance pattern mode.
3. The SDA acquires a 4MS trace at 20GS/s.

The following steps are done by a dll that implements SIGTEST algorithms:

4. Generate an eye pattern diagram from the data.
5. Compare with PCI Express transmit eye pattern specified for the probing location.
6. Compute the time between the jitter median and the maximum deviation from the median.

Values produced by SIGTEST are tested and included in the report individually.

Note: Mobile Graphics that are designed in accordance with the Mobile Graphics Low Power Addendum must have de-emphasis disabled.

Test 1.6: TX DC Common Mode Voltage

Assertions: PHY.3.1#12, PHY.3.1#26

Purpose: Measure TX DC Common Mode Voltage

Method:

1. Using the math functions of the SDA, measures the TX DC common mode voltage.
2. Measures the absolute delta of DC common mode voltage between D^+ and D^-.

This test should be done for all states.

Note: $V_{CM} = [V_{D+} + V_{D-}]/2$ (As defined in the PCI-Express Base Specification, Sec. 4.3.2).

Test 1.7: TX L0 to Electrical Idle to L0

Assertions: PHY.3.1#23, PHY.3.1#24, PHY.3.1#27

Purpose: TX Transition from L0 to Electrical Idle to L0

Method:

1. The SDA is set up to trigger when the transmitter transitions to electrical idle.
2. The user is asked to force the DUT transmitter to issue the Electrical Idle ordered-set and transition to Electrical Idle (In a Windows system, this can be accomplished by making Windows “Standby”).
3. The SDA verifies the DUT sends a K28.5 (COM) followed by three K28.3 (IDL) before entering Electrical Idle. It uses the 8B10B decode option to do this.
4. The SDA is used to verify that the transmitter is in a valid Electrical Idle state within 20 UI of the last symbol of the Electrical Idle ordered-set (or, if does not correctly send the EIOS, before dropping into Electrical Idle).

This test should be rerun while forcing the DUT to transition from L0 to Electrical Idle to L0 again using implementation-specific hardware or software methods in order to verify that the transmitter remains in Electrical Idle for a minimum of 50 UI. The QualiPHY script cannot automate that process.

Test 1.8: RX Detect Voltage

Assertion: PHY.3.1#14

Purpose: RX Detect - Maximum Voltage Change

Method: We measure the maximum change in voltage during receiver detection.

Test 1.9: RX Detect Hi-Z

Assertion: PHY.3.1#17

Purpose: RX Detection - High Receiver Impedance

Method:

1. Place 200 kΩ (Zrx-com-high-imp-dc Min) to ground in parallel with 3 nF on the transmitter data lines. During this step, the SDA is not connected to the DUT. Power on the DUT..
2. The SDA is connected to the DUT to verify that the associated TXs of the DUT did not enter CMM.

Test 1.10: RX Detect Low-Z

Assertion: PHY.3.1#18

Purpose: RX Detection - Low Receiver Impedance

Method:

1. Place 40 Ω (Zrx-com-dc Min) in series with 75 nF (Ctx Min) to ground on the transmitter data lines. During this step the SDA is not connected to the DUT. Power on the DUT.
2. The SDA is connected to the DUT to verify that the associated TXs of the DUT did enter CMM.

Test 1.11: Lane-to-Lane Skew

Assertion: PHY.3.3#8

Purpose: Lane-to-Lane Output Skew

Method:

1. Place all lanes of the device under test in compliance pattern mode.
2. Measure the bit-to-bit skew between all Lanes of the same Link. Ensure the measurement is made on equivalent data state transitions.

The script will repeat this test as many times as you want, to enable you to test skew between all lanes. In order to make sure that skew is measured in equivalent transitions the SDA looks for the entire compliance pattern. This test will therefore fail in a recognizable way if the DUT does not produce the correct compliance pattern. In that case, a message reflecting that will appear in the report.

Test 1.12: TX Output Rise/Fall

Assertion: PHY.3.3#3

Purpose: TX Output Rise/Fall Time

Method:

1. Connect 50 Ω loads to ground to the package pins of the silicon under test.
2. Place the silicon under test in polling compliance mode.
3. Measure the timing and voltage parameters within 0.2 inches of the package pins.

Note: This test is only intended to be done for TX; meaning, measured at the TX package pins.

If this test is done on System or Add-In card using the compliance test fixtures, it is guaranteed to pass because transition times are slowed down by coming through the PCIe connectors and several inches of traces on FR4. The results may be of interest but they do not indicate whether the TX would actually pass if tested at the package pins.

Note: For more accurate results, this measurement should be made using more than 6GHz of bandwidth - i.e. using an SDA 11000 or 13000.

Test 1.16: TX Transitions from Electrical Idle

Assertion: PHY.3.1#19

Purpose: TX Transitions from Electrical Idle

Method:

1. The script sets up the SDA to trigger when the transmitter transitions from electrical idle to sending differential data.
2. The user is prompted to force the DUT transmitter to leave Electrical Idle.
3. The script uses the SDA to verify that the DUT meets all TX differential signal specifications within 20 UI.

Note: Mobile Graphics that are designed in accordance with the Mobile Graphics Low Power Addendum must meet the transmitter eye requirements of the addendum.

Test 1.17: Receiver Detection Sequence

Assertions: PHY.3.1#30, PHY.3.1#31, PHY.3.1#32, PHY.3.1#33

Purpose: Receiver Detection Sequence

Method:

1. Set up the oscilloscope to trigger on the Receiver Detection sequence.
2. Verify that the transmitter starts at a stable voltage between VDD and GND prior to performing the common-mode shift.
3. If the common-mode voltage is equal to VDD, the shift must be towards GND.
4. If the common-mode voltage is equal to GND the shift must be towards VDD.
5. If the common-mode voltage is between VDD and GND the shift must be in the opposite direction the voltage moved to get to this initial common-mode voltage.

Test 1.18 Initial Active Link Training

Assertion: EM.2#27

Purpose: Measure the time between PERST de-assertion and the time that the link becomes active

Method:

1. The script sets up the SDA to trigger on the end of PERST#.
2. The script uses the SDA to measure the time from the end of PERST# to the initial active Link Training state (exit electrical idle).

Note: we have occasionally observed that turning on power to the system may cause a glitch on PERST that causes the SDA to trigger. The trigger level is at the appropriate level for detecting PERST. If that happens you can power down the system, press SINGLE on the SDA, and power on the system again before telling the script to continue; it will be clear on the SDA's display when it captures the rising edge of PERST instead of a glitch. Or, you can just allow it to fail and then use the script to repeat this test.

Test 1.19: Reference Clock Tests

These tests refer to Table 2-1 *REFCLK DC Specifications and AC Timing Requirements* in section 2.1.3 of the *PCI-Express Card Electromechanical Specification, Rev 1.1*.

Changes from Version 1.0a

Base Specification Changes:

- New clock recovery function for measuring eye diagrams

CEM Specification Changes:

- Reference clock specification and sample sizes
- Base Board measurement with unfiltered reference clock.

Single-Ended Tests

Input Voltage

Description:

REFCLK+ and REFCLK- must both be within the limits V_{MAX} and V_{MIN}, such that:

V_{MAX} = Absolute Max input voltage

= +1.15 V

V_{MIN} = Absolute Min input voltage

= -0.3 V

Where V_{MAX} is the maximum instantaneous voltage including overshoot, and V_{MIN} is defined as the minimum instantaneous voltage including undershoot (Figure 20, as follows).

Crossing Voltage

Description: V_{CROSS} Absolute

Crossing point voltage +250 to +550 mV

Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

V_{CROSS} Absolute refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing and refers to all crossing points for this measurement (Figure 20).

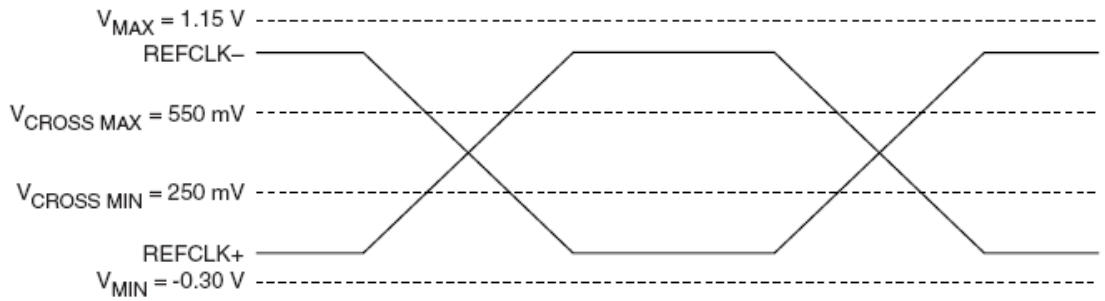


Figure 20. VCROSS Absolute (From PCI Express CEM 1.1 specification)

$V_{CROSS\ DELTA}$ = Variation of V_{CROSS} over all rising clock edges +140 mV

Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system (Figure 21).

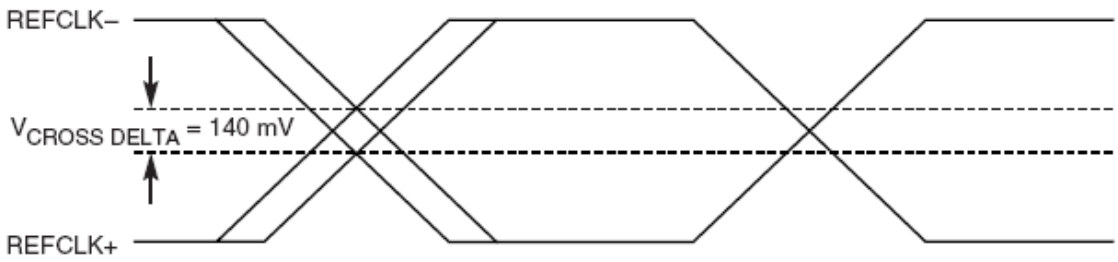


Figure 21. VCROSS Delta (From PCI Express CEM 1.1 specification)

Rise Fall Matching

Description: Rise-Fall Matching

Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching, max 20 %

Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where the rising edge of REFCLK+ meets the falling edge of REFCLK-. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 22 of the PCI-Express CEM 1.1 Specification.

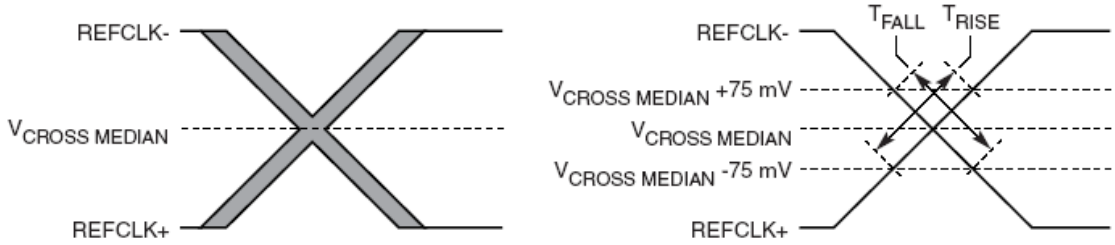


Figure 22. Rise-Fall Matching (From PCI Express CEM 1.1 specification)

Differential Tests

These tests can be made with Single Ended connections, the SDA will compute the difference C2-C3. We recommend using single ended connections.

Edge Rate

Description: Rise Edge Rate

Limits:

min = 0.6 GV/s

max = 4.0 GV/s

Description: Fall Edge Rate

Limits:

min = 0.6 GV/s

max = 4.0 GV/s

Test Condition: Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 23 of the PCI-Express CEM Specification, Rev 1.1.

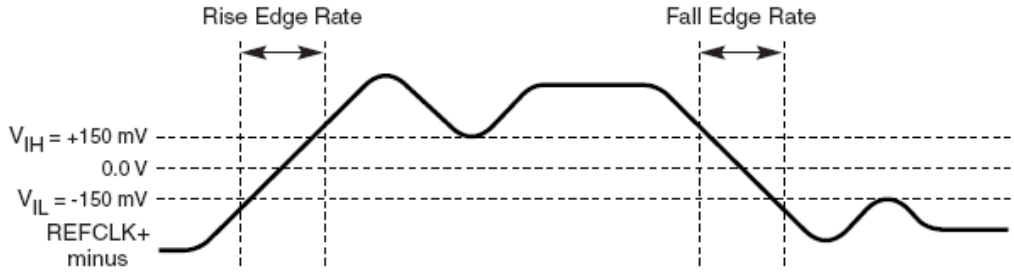


Figure 23. Fall Edge Rate (From PCI Express CEM 1.1 specification)

Differential Voltage

Description:

V_{IH} = Differential Input High Voltage

min = +150 mV

V_{IL} = Differential Input Low Voltage

max = -150 mV

Ringback

Description:

V_{RB} = Ring-back Voltage Margin

min = -100,

max = +100 mV

T_{STABLE} = Time before V_{RB} is allowed

max = 500 ps

Note: T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to drop back into the Vrb ±100 mV differential range. See Figure 24 of the PCI-Express CEM Specification, Rev 1.1.

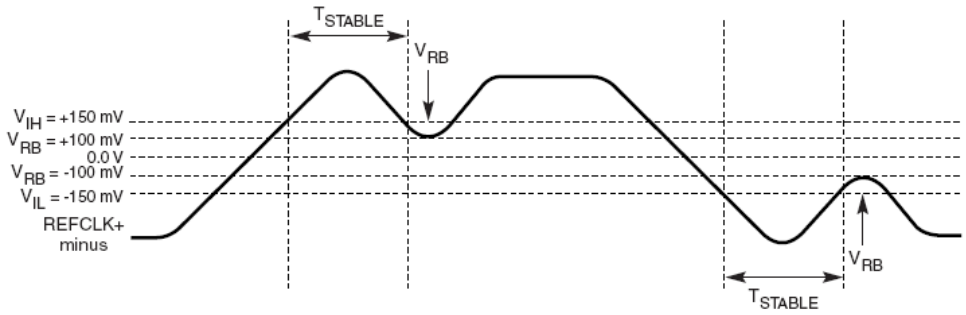


Figure 24. Ring Back (From PCI Express CEM 1.1 specification)

Period

Description:

$T_{PERIOD\ AVG}$ = Average Clock Period Accuracy

Limits:

min= -300 ppm

max = +2800 ppm

Note: PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 ppm, then, we have an error budget of 100 Hz/ppm * 300 ppm = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 ppm applies to systems that do not use Spread Spectrum, or that use common clock source. For systems employing Spread Spectrum there is an additional 2500 ppm nominal shift in maximum period resulting from the 0.5% down-spread, resulting in a maximum average period specification of +2800 ppm

$T_{PERIOD\ ABS}$ = Absolute Period (including Jitter and Spread Spectrum)

min = 9.847ns

max = 10.203 ns

Note: Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 25 of the PCI-Express CEM Specification, Rev 1.1.

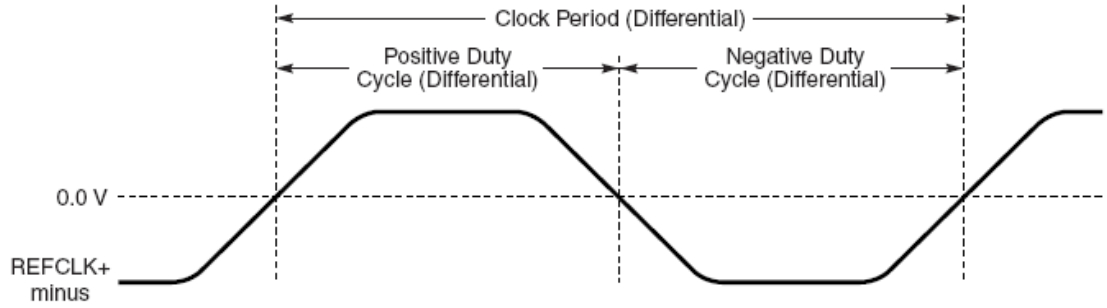


Figure 25. Period (from PCI Express CEM 1.1 specification)

Duty Cycle: min: 40%, max: 60%

- **SSC**

  Clock Period Accuracy min = -300 ppm, max = +2800 ppm

- **No SSC**

  Clock Period Accuracy min = -300 ppm, max = +300 ppm

§ § §